CIRCUIT AND METHOD FOR DETERMINING INTEGRATED CIRCUIT PROPAGATION DELAY

BACKGROUND OF THE INVENTION

Of all the tasks an integrated circuit (IC) designer faces, resolving timing violations, especially in large, complex IC designs, is one of the most onerous. This task is made difficult, in part, by the fact that IC logic gate delays can vary up to three times in response to changes in power supply voltage, operating temperature, and variations in the IC manufacturing process. Of these three variables, variations in process tend to dominate over changes in voltage and temperature, primarily because changes in the IC process for a particular IC remain constant once that IC has been manufactured. Voltage and temperature, on the other hand are changeable and, to a certain degree, controllable while the IC is operating.

The variations associated with IC process tend to affect a single IC in a more or less uniform manner, so relative differences in speed between multiple logic gates residing on a single IC are not particularly sensitive to those changes. However, input and output signals that couple the IC with other electronic circuits are especially susceptible to IC process variations, as an off-chip circuit with which the IC communicates is not likely to possess the same process variation as the IC. As a result, the relative changes in signal propagation times between the IC and other external circuits tend to be much greater than that between two internal signals of the IC. Such problems are often exacerbated in designs that involve multiple clock domains, in which multiple clocks of different frequencies and phases are utilized.

Currently, a couple of automatic techniques are often employed by IC designers to limit the effects of IC process variations to avoid signal timing problems. For example, an analog phase-locked loop (PLL) or a digital delay-locked loop (DLL) is often used to synchronize IC clock signals with external clock sources to counteract the negative effects of IC process variation. In other situations, process-

voltage-temperature (PVT) compensated input/output (I/O) pads for ICs have been utilized to combat the problem. However, circumstances often occur where neither of these techniques is available for a particular IC design, or the techniques cannot fully compensate for exceptional process variations.

Therefore, from the foregoing, a need currently exists for an alternative circuit or method that addresses the inherent problems associated with the manufacturing process variations of an integrated circuit.

SUMMARY OF THE INVENTION

As shown above, automatic compensation techniques are not always effective. Alternately, a more programmatic approach based on a determination of the extent of process variation in a particular IC may be more beneficial. More specifically, by somehow measuring the gate delay of an IC, that information may then be used in software executed on, for example, a microprocessor, to take effective action to counteract the process variation.

Embodiments of the invention, to be discussed in detail below, provide a circuit and method for determining the delay of an integrated circuit associated with chip-to-chip manufacturing process variations, voltage and temperature changes, and the like. First, a clock signal is inverted, thus generating an inverted clock signal, which is then delayed multiple times, resulting in several delayed versions of the inverted clock signal. Each version of the inverted clock signal is delayed a different length of time. The logical state of each delayed version of the inverted clock signal is then stored to provide an indication of the magnitude of the delay of the integrated circuit. Those stored logical states may then be employed to tune one or more critical signals to compensate for the observed propagation delays due to process, temperature, and voltage variations of the IC.

Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a circuit according to an embodiment of the invention.

FIG. 2 is an idealized timing diagram of the operation of the circuit of FIG. 1 given an integrated circuit exhibiting a faster-than-nominal propagation delay.

FIG. 3 is an idealized timing diagram of the operation of the circuit of FIG. 1 given an integrated circuit exhibiting a slower-than-nominal propagation delay.

FIG. 4 is a schematic diagram of a circuit according to a second embodiment of the invention.

FIG. 5 is a schematic diagram of a circuit according to an embodiment of the invention that may be employed in conjunction with the circuit of FIG. 1 to alter the propagation delay of a signal of the integrated circuit.

FIG. 6 is a flow chart of a method according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A schematic diagram of a circuit 100 according to an embodiment of the invention for determining IC signal propagation delay is shown in FIG. 1. First, using a clock signal CLK as input for the determining circuit 100, a logic inverter 102 is employed to generate an inverted clock signal 106.

The inverted clock signal 106 is used as a signal to be measured in determining the process-oriented delay of the IC. More specifically, the inverted clock signal 106 is provided as input to a number N of delay units 103 coupled together in a serial fashion. In the specific example of the determining circuit 100 of FIG. 1, each delay unit 103 consists of four inverters 105. An even number of inverters 103 may be used, depending on the particular circumstances involved. Also, other structures, such as delay lines, may be employed to perform essentially the same function. As a result, the output of each delay unit 103 generates a delayed inverted clock signal 107, which drives the next delay unit 103 in the series. Therefore, each delay unit 103 further along the series of delay units 103 produces a slightly more delayed version 107 of the inverted clock signal 106 than the immediately preceding delay unit 103.

In the specific example of FIG. 1, each delay unit 103 employs a substantially identical amount of delay, as evidenced by the equal number of inverters 105 within each unit 103. This structure is especially useful if the circuit propagation delays are linearly associated with variables such as temperature, voltage, and process-oriented variations of the IC. In alternate embodiments, that relationship may not be linear, but may instead be exponential, logarithmic, geometric, or another arithmetic relationship. In such cases, one or more delay units 103 may exhibit different propagation delays from other units 103 to more accurately describe those relationships.

In addition to each delay unit 103, a preliminary delay unit 104 located prior to the series of delay units 103 may also be employed to further delay each delayed inverted clock signal 107 by a uniform amount. This optional use of the preliminary delay unit 104 aids in positioning in time the transitions of the delayed inverted clock signals 107 compared to the original clock signal CLK, the importance of which is described below. The preliminary delay unit 104 may be positioned either before or after the logic inverter 102. As is the case with the delay units 103, the preliminary

delay unit 104 may be an even number of inverters 105 (as shown in FIG. 1), delay lines, or some other similar structure.

Each delayed inverted clock signal 107 generated by the delay units 103 drives the data input D of a logic storage element 108 of a first rank 110. Thus, each delay unit 103 has single logic storage element 108 of the first rank 110 with which it is associated. Further, each of the logic storage elements 108 of the first rank 110 is clocked by the original clock signal CLK by way of a clock input CK.

Given that each logic storage element 108 is driven by a slightly different delayed version 107 of the inverted clock signal 106, the possibility of at least one of the logic storage elements 108 of the first rank 110 encountering a timing violation between its delayed inverted clock signal 107 input and the clock signal CLK is not inconsequential. In other words, situations may occur in which the delayed inverted clock signal 107 for a particular logic storage element 108 is in transition between logic LOW and HIGH states at the same time that the clock signal CLK is also in transition. Such a situation may possibly cause the logic storage element 108 in question to become "metastable," which may cause the output of the storage element 108 to oscillate or hover at some voltage level between logic HIGH and LOW for an unacceptable period of time. To help prevent such problems, metastable-resistant flip-flops from the prior art may be employed for the logic storage elements 108 of the first rank 110.

To additionally address a potential metastability problem, a second rank 120 of logic storage elements 108 may be utilized to capture the outputs of the storage elements 108 of the first rank 110. In the specific embodiment of the determining circuit 100 of FIG. 1, the second rank 120 is clocked directly by the clock signal CLK, and the data inputs D are driven by the data outputs Q of the first rank 110 of logic storage elements 108. Alternately, if metastability problems are not anticipated at the data outputs Q of the first rank 110, the second rank 120 of logic storage elements 108 will not be necessary.

In the specific embodiment of FIG. 1, D-type flip-flops are employed as the logic storage elements 108 for both the first rank 110 and the second rank 120. Other types of logic storage elements, such as J-K and S-R flip-flops, may be employed as alternatives.

To facilitate discussion of the operation of the determining circuit 100, FIG. 2 and FIG. 3 show by way of timing diagrams how the circuit 100 operates within a faster-than-nominal IC and a slower-than nominal IC. In the fast case 200 shown in FIG. 2, the clock signal CLK and the inverted clock signal 106 (/CLK) are shown. Due to the action of the delay units 103, the state of each succeeding delayed inverted clock signal 107, each of which drives a data input D for each of the N logic storage elements 108 of the first rank 110, is delayed further by each delay unit 103. The waveforms for the data inputs D of the first rank 110 are numbered from D_{N-1} to D_0, aligning with the designation of the logic storage elements N-1 through 0 shown in FIG. 1. For an IC that exhibits a comparatively short propagation delay, each delay due to a delay unit 103 is accordingly short. As a result, each delayed inverted clock signal 107 is only delayed slightly compared to the preceding one. In this particular example, the leading edge of the clock signal CLK, shown by the vertical dotted lines of FIG. 2, clocks the logic level at the data inputs D into each logic storage element 108 of the first rank 110. Due to the short propagation delays, a logic HIGH value is clocked into a majority of the logic storage elements 108. Only after the effect of N-2 delay units 103 does the possibility of a logic LOW value being captured (at the data input D_2) into a logic storage element 108 of the first rank 110 exist. Assuming D_2 is interpreted as LOW, the resulting binary value captured collectively by the first rank 110 would be $D_{N-1}...D_0$ = 1111...1000. The fact that the first LOW value occurs toward the far right end of the captured data value indicates that the IC involved is faster than a nominally-processed IC.

If a second rank 120 of logic storage elements 108 is employed, as shown in FIG. 1, the values stored in the first rank 110 are available at the outputs of the second rank 120 one pulse of the clock signal CLK later.

FIG. 3 shows a slow case 201 in which a slower-than-nominal IC is involved. Again, the clock signal CLK and the inverted clock signal 106 (/CLK) are shown, along with the several delayed inverted clock signals 107 presented at the data input D of each logic storage element 108 of the first rank 110. However, in this particular case, a slower IC propagation delay results in each successive delayed inverted clock signal 107 being delayed a greater length of time from its predecessor. As a result, the first LOW value captured occurs in this case as early as the data input D_{N-4}. Also, as shown in FIG. 3, the later data inputs D may transition back to a logic HIGH. Other transitions may also be exhibited, depending on the number N of logic storage elements 108 residing in the first rank 110. However, the first transition from HIGH to LOW, which is at D_{N-4} in this instance, indicates that the IC propagation delay is longer than what may normally be expected.

To eliminate the possibility of multiple transitions in the values captured by the logic storage elements 108 of the first rank 110, a logic AND gate 109 associated with each delay 103 may be employed as shown in the second determining circuit 101 of FIG. 4. The output of each AND gate 109 is configured to drive the data input D of each logic storage element 108 of the first rank 110. The first input of each AND gate is configured to be driven by its associated delay unit 103, while the second input is fashioned to be driven by the output of the AND gate 109 associated with the previous delay unit 103 in the series. For the AND gate associated with the first of the series of delay units 103, the second input is held to a logic HIGH level. Use of the AND gates 109 serves to ensure that a logic LOW value for a delayed inverted clock signal 107 nulls out any potential HIGH logic levels from later delay units 103 in the series. As a result, the values captured by the logic storage elements 108 of the first rank 110 are thus essentially forced to represent a single HIGH-to-LOW transition.

In order for the determining circuit 100, 101 to operate well in all cases, some idea of the possible maximum and minimum propagation delays in the IC is helpful in order to determine an appropriate structure for the delay units 103. More specifically,

the number of delay units 103 and, hence, logic storage elements 108, to employ, as well as the delay associated with each delay unit 103, determine the total amount of delay that can be determined. For example, the total delay exhibited by all of the delay units 103 could be selected so that ICs exhibiting the shortest propagation delay would result in a timing violation or value transition from HIGH to LOW somewhere near the far right end of the series of delay units 103 (i.e., near data inputs D_1 or D_0). Additionally, the determining circuit 100 could also be structured so that ICs with the longest propagation delays would exhibit a HIGH-to-LOW transition as early as D_{N-1} or D_{N-2}. Also, the higher the number N of delay units 103, the more resolution in determining the relative propagation delay of the IC. Furthermore, the optional use of the preliminary delay unit 104 also helps determine where a possible timing violation is indicated within the N logic storage elements 108 of the first rank 110.

Furthermore, the determining circuit 100, 101 provides the added potential advantage of determining effects on IC propagation delay due to temperature and voltage variations while the IC is operating. Since the determining circuit 100, 101 does not specifically distinguish between the three identified sources of IC propagation delay variation, the determining circuit 100, 101 may be used to track any changes that occur during IC operation, not just those static propagation delays due to manufacturing process variation.

The determining circuit 100, 101 may be used in conjunction with a tuning circuit 300, as shown in FIG. 5, that uses the values from the determining circuits 100, 101 to tune the speed of a critical signal SIGNAL, such as a digital clock, typically by way of a programmable delay. For example, a microprocessor, microcontroller, application-specific IC (ASIC), or similar device 307 may be employed to read the outputs of the first rank 110 or second rank 120 of logic storage elements 108 by way of an addressable register, a general purpose port, or similar means. The microprocessor or similar device 307 may then tune the speed of one or more critical signals based on that output value. Similar to the determining circuit 100, 101, the tuning circuit 300 employs M serially-coupled delay units 305, each of

which in this case are comprised of several logic inverters 503. The output of each delay unit 305 drives the inputs of an M-to-1 multiplexer 310. As a result, each input of the multiplexer 310 is driven by a delayed version of the critical signal SIGNAL, with each version exhibiting a different propagation delay. One of the delayed versions is selected and transferred to the output DELAYED SIGNAL of the multiplexer 310 by way of $\log_2 M$ selector lines, which may be driven by an addressable register, a general purpose port, or similar means by the microprocessor 307. Thus, a critical signal may be delayed by some programmable amount depending on the overall IC propagation delay as determined by the determining circuit 100, 101, as described earlier.

The present invention also describes a method 400 for determining the propagation delay of an IC, as displayed in FIG. 6. Generally, a clock signal is logically inverted, resulting in an inverted clock signal (step 410). The propagation of that inverted clock signal is then delayed multiple times, resulting in several delayed inverted clock signals (step 420). Each of the delayed inverted clock signals is delayed a different amount. The logical state of each of the delayed inverted clock signals in then stored for each pulse of the original clock signal (step 430). As a result, the resulting stored states indicate the relative propagation delay of the IC. Optionally, that information may then be used to tune critical signals of the IC (step 440), as described above.

From the foregoing, specific embodiments of the invention provide a circuit and related method for determining the propagation delay associated with an integrated circuit. That circuit and method may then be used to tune critical signals of the IC to avoid timing problems resulting primarily from significant process variations, as well as temperature and voltage changes. Other embodiments of the present invention that are not specifically described herein are also possible. As a result, the invention is not to be limited to the specific forms so described and illustrated; the invention is limited only by the claims.